REMARKS/ARGUMENTS

Claims 6-25 are pending. Claims 6, 8-14, 16, 18-22, and 24 have been amended. No claim has been cancelled or added. No new matter has been added.

Claims 6-25 were rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu in view of Gill and Stewart. Applicants respectfully traverse the rejection. The claimed embodiment relates to a flash memory device that is configured for source-side programming. That is, a voltage is applied to a source region of a memory cell during a program operation, so that the hot electrons injected into the floating gate are provided by the drain region. In contrast, the conventional program operation applies a voltage to the drain region during the program operation, so that the hot electrons are provided by the source region.

The present inventors discovered that the source-side programming provides significant advantages over the conventional drain-side programming. One advantage is that the device can be programmed much faster. For example, Figs. 6 and 7 show that the source-side programming is almost three times faster than the drain-side programming. Also the threshold voltage distribution is much "tighter" for the source-side programming. See page 6, lines 24-29. As a result of the improved characteristics above, the channel length of the device may be made smaller than that for the conventional device. See page 6, lines 29-31. This enables the device to be made smaller, which is of primarily importance in today's semiconductor technology.

The claims herein are directed to flash memory devices are that configured for source-side programming. For example, the memory devices are provided with one or more of the following features: (1) the source region has a more graded profile than the drain region, (2) the source region has an upper doped region and a lower doped region, (3) the upper doped region of the source region is doped with arsenic and the lower doped region of the source region is doped with phosphorous, (4) the upper doped region of the source region has a doping concentration on the order of 10^{20} cm^{-3}, and (5) the gate/source overlap is greater than the gate/drain overlap.

The primary reference, Hsu, discloses a flash memory cell that uses the conventional drain-side programming method, as noted by the Examiner. The Examiner

attempts to use Stewart to remedy Hsu's deficiency. Applicants note that Stewart discloses a flash memory device with an entirely different structure than Hsu. Hsu discloses a flash memory device that is configured to optimize the device density. The source and drain regions are lines that are separated by a channel therebetween. This configuration enables millions of cells (or transistors) to be formed on a single die.

However, Stewart discloses a cell that comprises two rectangular regions, where each rectangular region defines a transistor. The cell of Stewart has the drain that is rectangular in shape. The channel/gate is provided around the perimeter of the drain. The source is provided around the perimeter of the channel/gate. That is, the drain, gate, and source all have rectangular shapes (or closed shapes). See col.2, lines 17-21 and Fig. 1.

Not only does Stewart requires two such rectangular structures for each cell, the closed-shape cell configuration is entirely unsuitable for the modern flash memory configuration, as disclosed in Hsu. The closed-shaped cell prevents the adjacent cells from sharing the drain and source regions. See Fig. 1B of Gill. In addition, the configuration of Stewart would negate an important benefit of the source-side programming, as discovered by the present inventors, i.e., the ability to more effectively reduce the cell size.

Accordingly, Applicants submit that there is no motivation to combine Hsu and Stewart. To establish a prima facie case of obviousness...there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinarily skilled in the art, to modify the reference or to combine reference teaching. MPEP 2143.

Applicants submit, without the benefit of hindsight and use of the present claims as a road map, Stewart would not suggest to those skilled in the art to adopt the device of Hsu for the source-side programming. In fact, Stewart teaches away from one of the primary goals of those skilled in the art, i.e., of reducing the cell size. Gill does not remedy the deficiency of Hsu and Stewart. Claim 6 is allowable at least for this reason.

In addition, Hsu discloses forming of a source region 124 (or N+ region) within a P-well 122. The drain region 118 (N+ region) is formed within a N- well 116. Accordingly, the

doping profile of the drain is more graded (or less abrupt) than the source, which is contrary to the device as claimed in claim 6.

Claim 14 recites, "...a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending into the substrate and having a first depth, the drain region having a first profile and being electrically coupled to a bit line extending in a second direction that is substantially perpendicular to the first direction; and a source region provided in the substrate and proximate a second end of the floating gate, the source region and drain region defining a channel therebetween, the source region extending into the substrate and having a second depth that is greater than the first depth, the source region having a second profile, wherein the first profile of the drain region has a more abrupt profile than the second profile of the source region, wherein the control gate is applied with a first voltage of 8.5 volts or less and the source region is applied with a second voltage of 4.5 volts or less to program the non-volatile device, wherein the floating gate, control gate, drain region, and source region together define a first memory cell, wherein the non-volatile device further includes a second memory cell including a source region that shares a common node with the source region of the first memory cell." None of the cited references disclose the above features. Claim 14 is allowable.

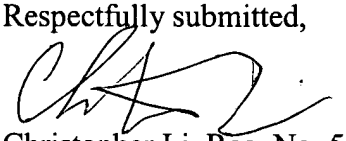
Claim 19 recites, "a drain region provided in the substrate and proximate a first end of the floating gate, the drain region extending a first distance into the substrate and having a first profile relative to the substrate, the drain region being electrically coupled to a second conductive line extending in a second direction that is substantially perpendicular to the first direction, and a source region provided in the substrate and proximate a second end of the floating gate, the source region being a double-diffused region that extends a second distance into the substrate and having a second profile relative to the substrate, the second distance being greater than the first distance, wherein the control gate is applied with a first voltage of no more than 8.5 volts and the source region is applied with a second voltage of no more than 4.5 volts to program the non-volatile device, wherein the memory cell is defined by a single transistor." None of the cited references disclose the above features. Claim 19 is allowable.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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